SiGe/Si SUPERLATTICE COOLERS

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ABSTRACT

The fabrication and characterization of SiGe/Si superlattice coolers are described. Superlattice structures were used to enhance the device performance by reducing the thermal conductivity between the hot and the cold junctions, and by providing selective removal of hot carriers through thermionic emission. Cooling of 2.2 K and 2.5 K were measured on n-type and p-type 75 × 75 μm^2 devices, corresponding to cooling power densities of hundreds of watts per square centimeter. Cooling up to 7.2 K was obtained at 150 °C for p-type 50 × 50 μm^2 devices. The results show that n-type and p-type coolers can work together in similar optimal conditions. This paves the road to fabricate n-type and p-type superlattice coolers in an array format electrically in series and thermally in parallel, similar to conventional thermoelectric devices, and thus achieve large cooling capacities with relatively small currents.

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INTRODUCTION

The demand for high-speed, high-density very-large-scale integrated (VLSI) circuits is accompanied by higher power densities. Many devices are already operating at or near the edge of their reliability. Heat generation and thermal management are becoming one of the barriers to further increase clock speeds and decrease feature sizes. Thermoelectric (TE) refrigeration is a solid-state active cooling method with high reliability. TE coolers are silent, environmentally "green" and capable for spot cooling. Bi_2Te_3 based TE coolers are commonly used in electronics and optoelectronics for cooling and temperature stabilization, but their manufacturing is a bulk technology and is incompatible with integrated circuit (IC) fabrication process. Solid-state coolers monolithically integrated with VLSI devices are an attractive way to achieve compact and efficient cooling. However, the TE figure of merit (Z) is quite low for most of the semiconductors used in microelectronics and optoelectronics. This makes it difficult to get high performance integrated coolers. Recently heterostructure thermionic coolers and superlattice coolers are proposed, and theoretical calculations show that large improvement in Z can be achieved and efficient cooling becomes possible with coolers made of conventional semiconductor materials [1-6]. InP based heterostructure integrated thermionic coolers have been demonstrated by Shakouri et al, one degree cooling was obtained over 1 μm InGaAsP barrier [7-8]. In this paper, we report our experimental results for SiGe/Si superlattice coolers.

SiGe is a good thermoelectric material for high temperature refrigeration and power generation applications [9]. It has been used for thermo-nuclear power generation in satellites for deep space missions. In this paper we describe the fabrication and characterization of single-element SiGe/Si superlattice coolers that use thermionic and thermoelectric effects. Both n-type and p-type devices have been demonstrated. This paves the road to fabricate n-type and p-type superlattice coolers in an array format electrically in series and thermally in parallel, similar to conventional thermoelectric devices, and thus achieve large cooling capacities with relatively small currents. Superlattice structures can enhance the cooler performance by reducing the thermal conductivity between the hot and the cold junctions [10] and by selective emission of hot carriers above the barrier layers in the thermionic emission process [1-2, 7]. Si and SiGe-based devices can be monolithically integrated with these coolers to achieve better device performance.

MATERIAL AND DEVICE FABRICATION

SiGe/Si superlattice structures were grown in a Perkin-Elmer Si molecular beam epitaxy (MBE) growth chamber on 125 mm diameter, (001)-oriented Si substrates doped to <0.020 Ω-cm with Sb for the n-type devices and to <0.006 Ω-cm with B for the p-type devices.

The cooler's main part is a 3 μm thick $Si_{0.7}Ge_{0.3}$/Si superlattice grown symmetrically strained on a buffer layer designed so that the in-plane lattice constant approximates that of relaxed $Si_{0.9}Ge_{0.1}$. The doping levels are 2×10^{19} cm^{-3} and 5×10^{19} cm^{-3} for n-type and p-type SiGe/Si superlattices, respectively.

For the relaxed buffer layer, we grew a 10-layer structure, alternating between 150 nm $Si_{0.9}Ge_{0.1}$ and 50 nm $Si_{0.845}Ge_{0.150}C_{0.005}$, roughly following the method suggested by Osten et al. [11]. For the n-type sample, the layers were grown at 390 °C and annealing was performed at 750 °C for 10 minutes after the growth of each $Si_{0.9}Ge_{0.1}$ layer. In the p-type case, the growth temperature was simply alternated between 700 °C for the $Si_{0.9}Ge_{0.1}$ layer and 500 °C for the $Si_{0.845}Ge_{0.150}C_{0.005}$ layer. After the relaxed buffer sequence, another 150 nm thick $Si_{0.9}Ge_{0.1}$ layer was grown at 390 °C for the n-type sample and a 1 μm thick $Si_{0.9}Ge_{0.1}$ layer was grown at 700 °C for the p-type case. Growth of a 200 period, 5 nm $Si_{0.7}Ge_{0.3}$/ 10 nm Si superlattice then followed at 390 °C (n-type case) and 500 °C (p-type case). Finally, the samples were capped with a heavily doped $Si_{0.9}Ge_{0.1}$ layer sequence to provide for a low-resistance ohmic contact.

The processing of SiGe/Si superlattice coolers is compatible with that of VLSI technology. Mesas 3.6 μm high were fabricated using reactive ion etching down to the SiGe buffer layer to form the devices. Metallization was made on the mesa and $Si_{0.9}Ge_{0.1}$ buffer layer for top and bottom contact respectively. A scanning electron microscope (SEM) image of the processed devices is shown in Fig. 1.

Electrical contact resistance is an important factor that limits the optimum device performance. Low contact resistance is essential for thin film coolers [12]. A 100 nm titanium metal layer was first deposited. This was intended to form a titanium silicide on the silicon surface and to act as a metal barrier to separate Si and Al. Subsequently 1 μm thick aluminum layer was deposited. To facilitate wire bonding, an additional metal layer of titanium and gold was used. Annealing was accomplished at temperatures between 400 °C and 600 °C with rapid thermal annealer. TLM (transmission line mode) measurements were carried out to measure the contact resistance. The measured specific contact resistivity is in the mid 10^{-7} Ω-cm^2 range for both n-type and p-type devices as shown in Fig. 2.

TEST RESULTS AND DISCUSSIONS

As shown in Fig. 3, the SiGe/Si superlattice coolers were tested on a temperature controlled copper plate that worked as the heat sink. The heat sink is set at a constant temperature during the device testing. To cool the top of the devices, current was sent from the top metal contact to bottom metal contact for p-type device and the reverse direction for n-type device. Micro thermocouples were used to measure the cooling temperatures. Fig. 4 displays the measured temperature on top of the 75×75 μm^2 n-type and p-type devices as a function of current with the heat sink at 25 °C. The cooling temperature is relative to the value at zero current. Despite the large thermal resistance of the Si substrate and package on the hot side of the cooler and Joule heating in the wires connected to the cold junction, a net cooling of 2.2 K and 2.5 K was observed on top of the n-type and p-type devices respectively. This cooling over the small barrier thickness corresponds to cooling capacities on the order of hundreds of watts per square centimeter.

Devices of different sizes, from 50×50 μm^2 to 150×150 μm^2, were tested. The results on p-type SiGe/Si coolers are shown in Fig. 5. 2.7 K cooling is obtained for the 50×50 μm^2 p-type device. The test results shows the maximal cooling temperature increases as the device size decreases. This cannot be explained with conventional ideal thermoelectric or thermionic cooler models. This is due to the three-dimensional (3D) nature of current spreading in the substrate and

the Joule heating from the bonding wires. For the same wire resistance, smaller devices require a smaller optimum current which is favorable for better cooling performance. A 3D finite-difference heat equation solver [8] is being used to model the device performance.

The SiGe/Si superlattice coolers have a better performance at higher temperatures. The measured cooling for 50×50 μm^2 p-type SiGe/Si devices at 150 °C (heat sink temperature) is shown in Fig. 6. The net cooling increases from 2.7 K at 25 °C to 7.2 K at 150 °C. The reason for improved performance with the increase in temperature is two fold. First, in the temperature range of our measurements, the figure of merit ZT of SiGe alloy increases with temperature due to smaller thermal conductivity and larger Seebeck coefficient at higher temperatures [13], and second, the thermionic emission cooling power increases due to the larger thermal spread of carriers near the Fermi energy.

Since the devices described above are single element superlattice coolers, heat conduction to the cooling side from the bonding wires or probes are unavoidable. This reduces the maximum cooling. To solve this problem, n-type and p-type SiGe/Si superlattice coolers can be made in an array format electrically in series and thermally in parallel, similar to conventional thermoelectric coolers. In this way, both electrical terminals can be made at the heat sink side, and large cooling capacities can be achieved with relatively small currents. For the cooler array, it is preferable to have n-type and p-type devices work at the same optimal current. This can be done by selecting suitable device sizes for the cooler couple. For example, optimal operation currents for the n-type 75×75 μm^2 devices (in Fig. 4) and the p-type 50×50 μm^2 devices (in Fig. 5) are about the same, cooling of 2.2 K and 2.7 K can be obtained at the same current ~230 mA.

With optimized superlattice material and device design and packaging, cooling up to tens of degrees is possible. More important, the processing of SiGe/Si superlattice coolers is compatible with that of VLSI technology, thus it is possible to integrate these coolers monolithically with Si and SiGe devices to achieve compact and efficient cooling.

CONCLUSIONS

SiGe/Si superlattice coolers were demonstrated and cooling of 2.2 K and 2.5 K were measured for n- and p-type 75×75 μm^2 devices. Cooling up to 7.2 K was obtained at 150 °C for p-type 50×50 μm^2 devices. The results show that the packaged devices of both n- and p-type coolers can work together with similar bias current conditions. This paves the road to fabricate n- and p-type superlattice coolers in an array format electrically in series and thermally in parallel, similar to conventional thermoelectric devices. Thus large cooling capacities with relatively small currents can be achieved and the problems of series resistance and heat load of contacting wires can be avoided.

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FIGURE CAPTIONS

Figure 1. SEM image of the processed SiGe/Si superlattice cooler devices.

Figure 2. Ohmic contact resistance for n-type and p-type SiGe based on TLM measurements. The doping is 2×10^{20} cm^{-3} for p-type SiGe and 1×10^{20} cm^{-3} for n-type SiGe.

Figure 3. Schematic diagram of SiGe/Si superlattice cooler for testing (not to scale).

Figure 4. Measured cooling for n-type and p-type 75×75 μm^2 SiGe/Si superlattice coolers at 25 °C heat sink temperature.

Figure 5. Cooling measured on top of p-type SiGe/Si superlattice coolers of different sizes at 25 °C heat sink temperature.

Figure 6. Measured cooling for a 50×50 μm^2 p-type SiGe/Si superlattice cooler at 150 °C heat sink temperature.

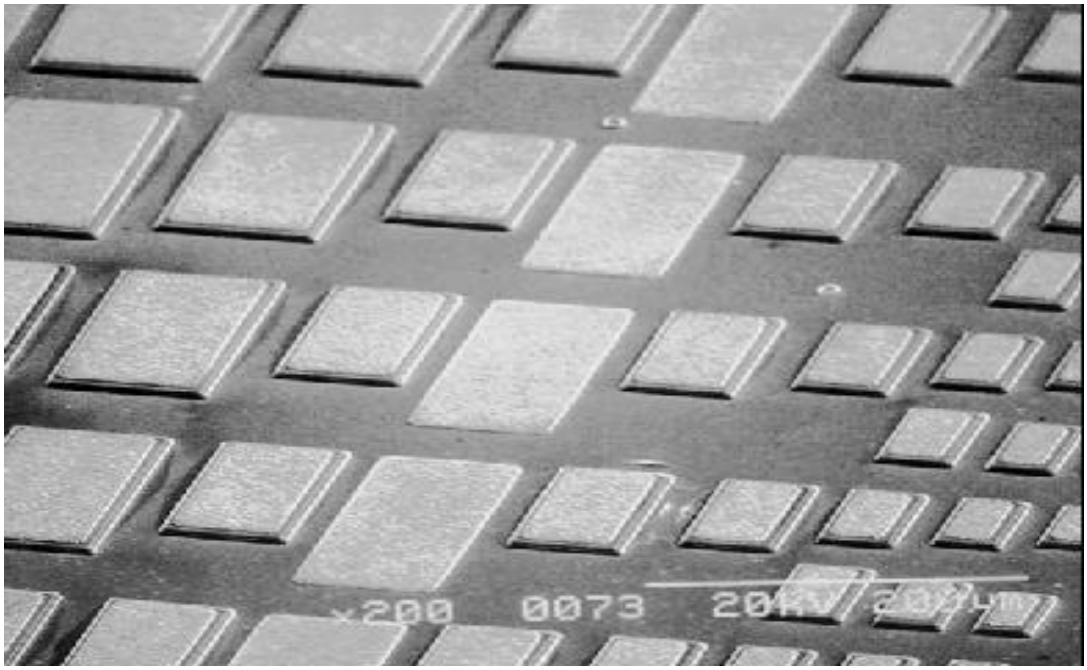

Fig. 1

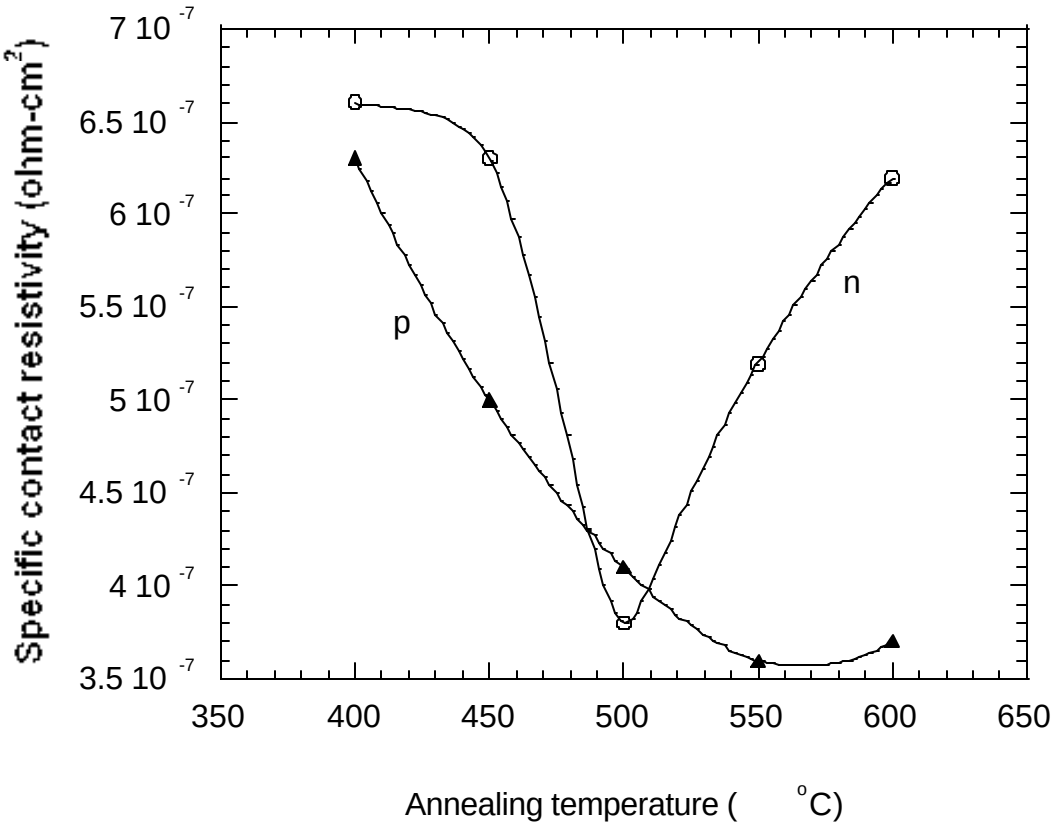
Specific contact resistivity (ohm-cm^2)
7 10^{-7}
6.5 10^{-7}
6 10^{-7}
5.5 10^{-7}
5 10^{-7}
4.5 10^{-7}
4 10^{-7}
3.5 10^{-7}
350
400
450
500
550
600
650
p
n
Annealing temperature (^{o}C)

Fig. 2

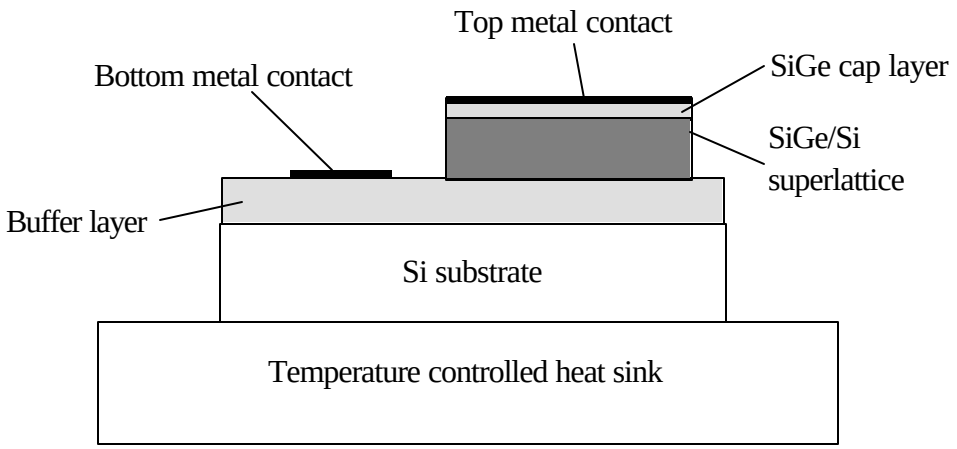
Top metal contact
Bottom metal contact
SiGe cap layer
SiGe/Si
superlattice
Buffer layer
Si substrate
Temperature controlled heat sink

Fig. 3

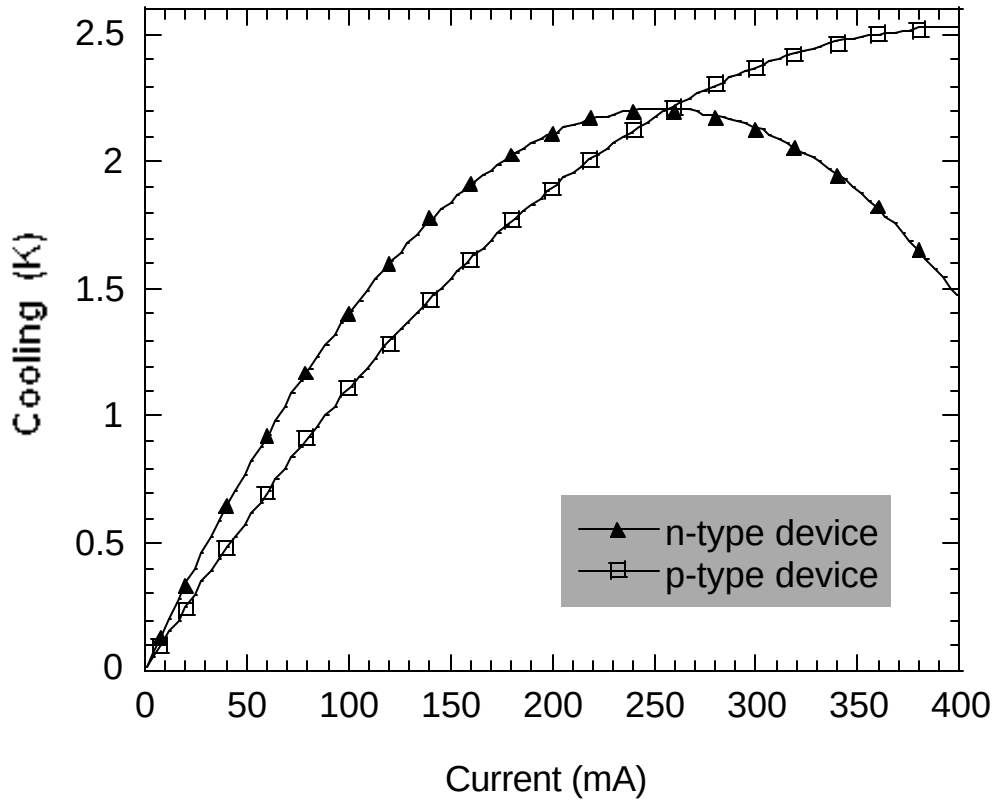
Cooling (K)
Current (mA)
n-type device
p-type device
0
0.5
1
1.5
2
2.5
0
50
100
150
200
250
300
350
400

Fig. 4

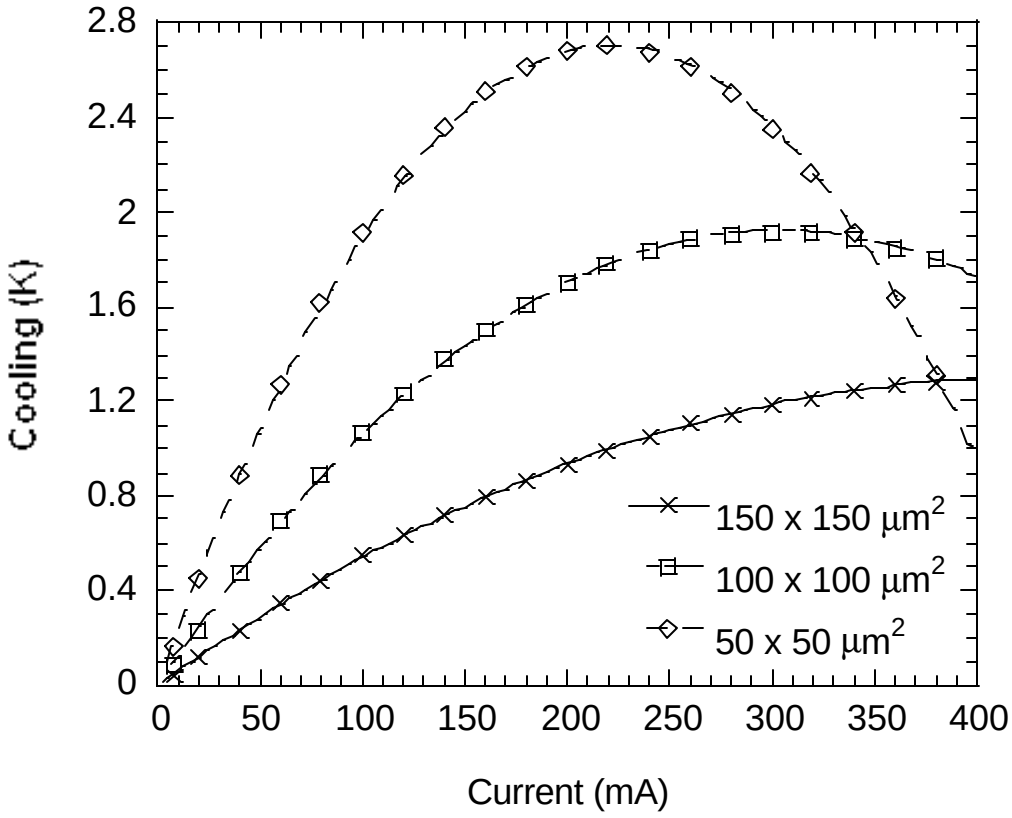
Cooling (K)
Current (mA)
0
0.4
0.8
1.2
1.6
2
2.4
2.8
0
50
100
150
200
250
300
350
400
150 x 150 μm2
100 x 100 μm2
50 x 50 μm2

Fig. 5

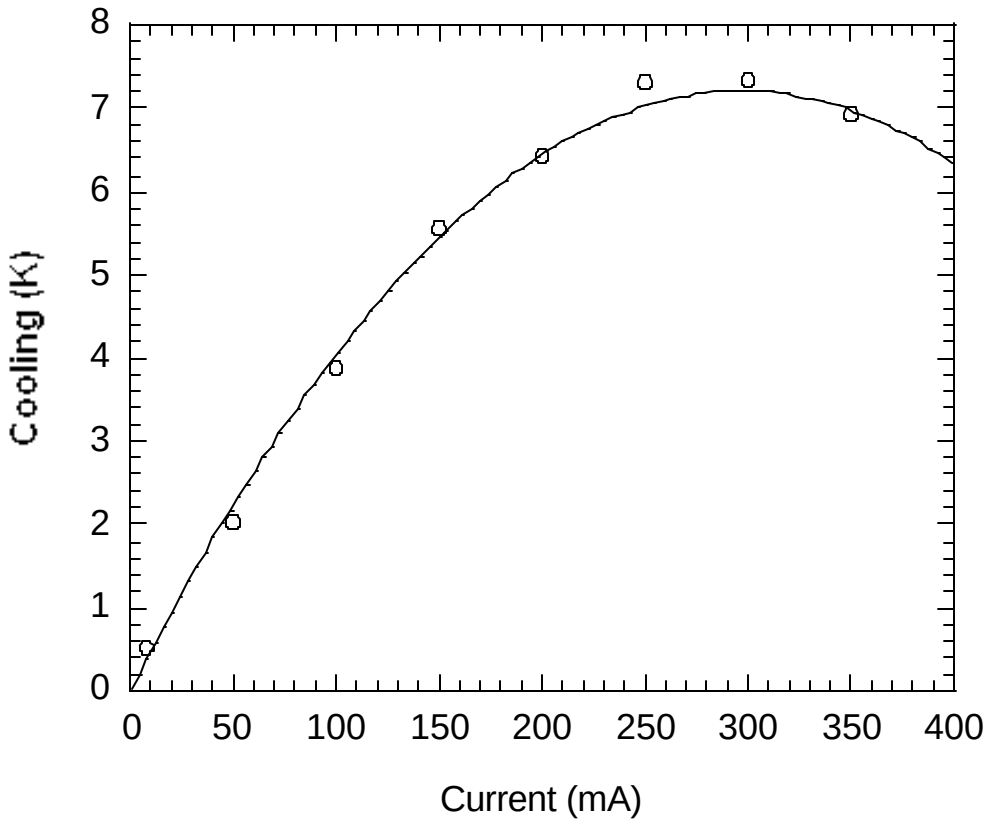
Cooling (K)
Current (mA)
0
1
2
3
4
5
6
7
8
0
50
100
150
200
250
300
350
400

Fig. 6